CLAIMS:

1. A method of forming a structure over a semiconductor substrate, comprising:

forming a silicon dioxide containing layer across at least some of the substrate;

providing nitrogen within the silicon dioxide containing layer, substantially all of the nitrogen within the silicon dioxide being at least 10Å above the substrate; and

after providing the nitrogen within the silicon dioxide containing layer, forming conductively doped silicon on the silicon dioxide layer.

2. The method of claim 1 wherein the silicon dioxide layer is at least 30Å thick, and wherein substantially all of the nitrogen is provided in the top 10Å of the silicon dioxide layer.

3. The method of claim 1 wherein the nitrogen is provided within the silicon dioxide layer from plasma activated nitrogen species.

4. The method of claim 1 wherein the nitrogen is provided within the silicon dioxide layer by remote plasma nitridization utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate.

5. The method of claim 1 wherein the nitrogen is provided within the silicon dioxide layer by remote plasma nitridization utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate; the plasma being generated in a chamber from N_2, at a power of from about 1500 watts to about 3000 watts, and a pressure of from about 0.5 Torr to about 3 Torr; the substrate not being biased relative to the plasma during provision of the nitrogen within the silicon dioxide layer.

6. The method of claim 5 wherein the substrate is maintained at a temperature of from about 550°C to about 1000°C during provision of the nitrogen within the silicon dioxide layer.

7. The method of claim 5 wherein the substrate is exposed to the nitrogen species for a time of from greater than 0 minutes to about about 5 minutes.

8. The method of claim 1 wherein the nitrogen is provided within the silicon dioxide layer by plasma nitridization utilizing nitrogen species generated in a plasma that is at least about 4 inches from the substrate.

9. The method of claim 8 wherein the substrate is maintained at a temperature of from about 550°C to about 1000°C during provision of the nitrogen within the silicon dioxide layer.

10. The method of claim 8 wherein the substrate is exposed to the nitrogen species for a time of from greater than 0 minutes to about about 5 minutes.

11. A method of forming structures over a semiconductor substrate, comprising:

forming a first oxide region which covers only a portion of the substrate;

providing nitrogen within the first oxide region, substantially all of the nitrogen within the first oxide region being at least 10Å above the substrate;

forming a second oxide region over at least some of the substrate which is not covered by the first oxide region;

forming a first conductively-doped silicon material over the first oxide region and a second conductively-doped silicon material over the second oxide region; one of the first and second conductively-doped silicon materials being n-type doped and the other being p-type doped.

12. The method of claim 11 wherein the nitrogen is provided within the first oxide region from plasma activated nitrogen species.

13. The method of claim 11 wherein the second oxide region is thicker than the first oxide region.

14. The method of claim 11 wherein the p-type doped silicon material is formed over the first oxide region.

15. The method of claim 11 wherein the p-type doped silicon material is formed over the first oxide region, and is formed before forming the second oxide region.

16. The method of claim 15 wherein the second oxide region is formed by oxidizing the substrate, and wherein the oxidizing also oxidizes the p-type doped silicon material to form a third oxide region over the p-type doped silicon material.

17. The method of claim 11 wherein:

the p-type doped silicon material is formed over the first oxide region, and is formed before forming the second oxide region;

the second oxide region is formed by oxidizing the substrate, and wherein the oxidizing also the oxidizes the p-type doped silicon material to form a third oxide region over the p-type doped silicon material; and

the n-type doped silicon material is formed over the second and third oxide regions.

18. The method of claim 17 further comprising removing the n-type doped silicon material and third oxide layer from over the p-type doped silicon material.

19. The method of claim 17 further comprising removing the n-type doped silicon material and third oxide layer from over the p-type doped silicon material by chemical-mechanical planarization.

20. The method of claim 17 further comprising:

removing the n-type doped silicon material and third oxide layer from over the p-type doped silicon material;

patterning the p-type doped silicon material into a first transistor gate;

patterning the n-type doped silicon material into a second transistor gate;

forming first source/drain regions proximate the first transistor gate to define a first transistor comprising the first source/drain regions and first transistor gate; and

forming second source/drain regions proximate the second transistor gate to define a second transistor comprising the first source/drain regions and first transistor gate.

21. A method of forming a pair of transistors associated with a semiconductor substrate, comprising:

defining a first region and a second region of the substrate;

forming a first oxide region which covers at least some of the first region of the substrate and which does not cover the second region of the substrate;

providing nitrogen within the first oxide region;

after providing the nitrogen within the first oxide region, forming a first conductive layer over the first oxide region and which does not cover the second region of the substrate;

after forming the first conductive layer, forming a second oxide region over the second region of the substrate;

forming a second conductive layer over the second oxide region;

patterning the first conductive layer into a first transistor gate;

patterning the second conductive layer into a second transistor gate;

forming first source/drain regions proximate the first transistor gate and gatedly connected to one another by the first transistor gate; and

forming second source/drain regions proximate the second transistor gate and gatedly connected to one another by the second transistor gate.

22. The method of claim 21 wherein the second oxide region is thicker than the first oxide region.

23. The method of claim 21 wherein the first and second conductive layers comprise conductively doped silicon.

24. The method of claim 21 wherein the first and second conductive layers comprise conductively doped silicon, the first conductive layer comprising p-type doped silicon and the second conductive layer comprising n-type doped silicon.

25. The method of claim 21 wherein the first and second conductive layers comprise conductively doped silicon, wherein the substrate is oxidized to form the second oxide region, and wherein the first conductive layer is oxidized during formation of the second oxide region.

26. The method of claim 21 wherein the first and second conductive layers comprise conductively doped silicon, wherein the substrate is oxidized to form the second oxide region, wherein the first conductive layer is oxidized during formation of the second oxide region, wherein the second conductive layer is formed over the oxidized first conductive layer; and wherein the second conductive layer is removed from over the oxidized first conductive layer prior to patterning the first conductive layer into a transistor gate.

27. The method of claim 21 wherein the nitrogen is provided within the first oxide region from plasma activated nitrogen species.

28. The method of claim 21 wherein the second oxide region is thicker than the first oxide region.

29. The method of claim 21 wherein the p-type doped silicon material is provided over the first oxide region.

30. The method of claim 21 wherein the p-type doped silicon material is formed over the first oxide region, and is formed before forming the second oxide region.

31. The method of claim 21 wherein the substrate comprises monocrystalline silicon and the oxide regions comprise silicon dioxide; and wherein the first and second oxide regions are grown from the monocrystalline silicon substrate.

32. A semiconductor assembly, comprising:

a semiconductor substrate having a first region and a second region defined therein;

a first oxide region on the substrate and covering the first region of the substrate; the first oxide region having nitrogen provided therein; substantially all of the nitrogen being at least 10Å above the semiconductor substrate;

a first conductive layer over the first oxide region and defining a first transistor gate;

first source/drain regions proximate the first transistor gate and gatedly connected to one another by the first transistor gate; and

a second oxide region covering the second region of the substrate;

a second conductive layer over the second oxide region and defining a second transistor gate;

second source/drain regions proximate the second transistor gate and gatedly connected to one another by the second transistor gate.

33. The assembly of claim 32 wherein substantially all of the nitrogen is within a top 10Å of the first oxide region.

34. The assembly of claim 32 wherein the second oxide region is thicker than the first oxide region.

35. The assembly of claim 32 wherein the first conductive layer comprises p-type doped silicon and the second conductive layer comprises n-type doped silicon.